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Model Predictive Controller with Reduced Complexity for Grid Tied Multilevel Inverters

Soumya Ranjan Mohapatra and Vivek Agarwal, *Fellow IEEE*

***Abstract*— Finite control set model predictive control (FCSMPC) has become popular for grid interactive applications due to its simplicity and ease of implementation. Since the implementation of FCSMPC requires all possible Switching States (SS) of the inverter, the computational burden is an important issue, which needs to be addressed while applying FCSMPC to the control of multilevel inverters. This paper proposes a novel 'S' factor scheme for the FCSMPC implementation, which reduces complexity while controlling grid current and balancing the capacitor voltages in neutral point clamped three-level inverters. The proposed scheme is very easy to implement and can be extended to any higher level inverter without any additional effort. In this method, at every sampling instant, redundant SS are chosen suitably and the predicted reference inverter voltage (PRIV) vector is derived from predicted grid voltage, predicted reference current and the present value of the actual current. Subsequently, 'S' factor scheme is applied to select the switching state, which is close to PRIV vector. The selected switching state is then applied at the same sampling instant. The proposed scheme is experimentally compared with a recent FCSMPC algorithm to validate the performance.**

***Index Terms*— Calculation burden, Finite control set model predictive control, Grid interactive systems, Multi-level inverter, 'S' factor scheme.**

I. INTRODUCTION

THE popularity of multilevel inverters in high power grid-interactive industry applications is growing by the day. A wide range of control algorithms and topologies has been developed by researchers to improve the performance of multilevel inverters [1]. The power circuit of the basic three level Neutral Point Clamped (NPC) grid connected Voltage Source Inverter (VSI) is depicted in Fig. 1. The conventional linear controllers with space vector modulation used for such VSIs have several drawbacks such as stability issues, gain parameter tuning, unsatisfactory transient performance, etc. [2].

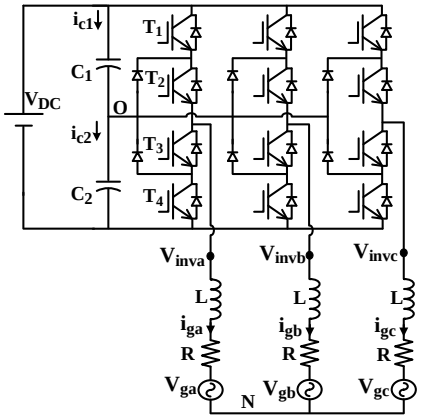

Fig. 1.The power circuit of a grid connected three level NPC VSI

In recent years, the advancements in digital computing technology have led many researchers to focus on the finite control set model predictive control (FCSMPC) of grid interactive systems [3-6]. As the FCSMPC takes advantage of finite number of Switching States (SS) in multilevel inverters, it is simple to understand and easy to implement [5]. A major shortcoming of the FCSMPC, however, is its computational burden which increases with the number of SS. Therefore, special attention needs to be given to reduce computational burden while applying FCSMPC to multilevel VSIs, since they have a higher number of SS.

Various optimization methods which give superior performance under long prediction horizons introduces complexity in FCSMPC [6,7]. Cortes et al. have proposed FCSMPC for cascaded H-bridge multilevel inverters by eliminating redundant voltage vectors [8]. They further reduced the calculation burden by taking a subset of adjacent voltage vectors for evaluating the cost function. However, the transient performance is hampered by considering only a subset of voltage vectors. A new concept [9,10] to reduce the calculation burden is proposed by splitting the optimization problem into two parts. First, the optimal voltage level is identified, and then the redundant voltage vector that gives the best optimal solution is determined. However, all the above methods [8-10] are based on current predictions, which require a higher number of predictions.

Simpler and computationally efficient reference inverter voltage vector prediction based FCSMPCs have been proposed for NPC multilevel VSIs in [11-14]. In these papers,

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S. R. Mohapatra and V. Agarwal are with the Indian Institute of Technology Bombay, Mumbai 400076, India (e-mail: soumyaranjan597@gmail.com; agarwal@ee.iitb.ac.in).

the Neutral Point Voltage (NPV) of the inverter is controlled by adding another term with less priority in the cost function which is supposed to control only grid current. The priority level of controlling the NPV is decided by a weighing factor. However, there is yet no well-established rule for tuning the weighing factor, and the addition of this extra term in the cost function also hampers the THD of the grid current [5]. Sector identification is incorporated in [14] to reduce the number of cost function evaluations for controlling the grid current and the NPV.

This paper reports a novel 'S' factor scheme in which the optimal voltage vector is obtained to control the grid current and the NPV without the need of evaluating any cost function. The proposed 'S' factor scheme has the following advantages over the existing schemes:

(a) This scheme reduces the overall execution time since it has fewer calculations to perform as compared to other conventional FCSMPC available in the literature.

(b) This scheme completely avoids any tuning parameter to control NPV

(c) The THD of grid current remains unaffected.

(d) This scheme can also be easily generalized for any higher-level inverter.

II. Controller Design

The dynamic model of a three-level inverter shown in Fig.1 plays an essential role in designing the FCSMPC, and it is given by:

$$\frac{d\vec{i}_g}{dt} = \frac{1}{L}(-R\vec{i}_g + \vec{v}_{inv} - \vec{v}_g) \quad (1)$$

where $\vec{v}_{inv} = \left[v_{invx} v_{invy}\right]^T$, $\vec{i}_g = \left[i_{gx}\ i_{gy}\right]^T$ and $\vec{v}_g = \left[v_{gx} v_{gy}\right]^T$ are the VSI voltages, the grid currents, and grid voltages respectively. The voltages and currents, having subscripts 'x' or 'y' indicate that the quantities have been obtained from their original values using Clarke's transformation. The predicted grid current at the next sampling instant, which is calculated by discretizing (1) is given by [15]:

$$\vec{i}_g(n+1) = \frac{1}{RT_s + L}\{L\vec{i}_g(n) + T_s[\vec{v}_{inv}(n+1) - \vec{v}_g(n+1)]\} \quad (2)$$

where the sampling time is denoted by 'T_s' and the sampling instant by.'n' Rearranging (2), one can get

$$\vec{v}_{inv}(n+1) = \frac{RT_s + L}{T_s}\vec{i}_g(n+1) - \frac{L}{T_s}\vec{i}_g(n) + \vec{v}_g(n+1) \quad (3)$$

$\vec{i}_g(n+1)$ can be replaced by $\vec{i}_g^*(n+1)$ to get the predicted reference inverter voltage (PRIV) vector [11-15] as follows:

$$\vec{v}_{inv}^*(n+1) = \frac{RT_s + L}{T_s}\vec{i}_g^*(n+1) - \frac{L}{T_s}\vec{i}_g(n) + \vec{v}_g(n+1) \quad (4)$$

From (4), it is clear that the PRIV vector can be derived from the predicted reference current $\vec{i}_g^*(n+1)$, the predicted grid voltage $\vec{v}_g(n+1)$ and the present value of the actual grid current $\vec{i}_g(n)$. The predicted grid voltage and the predicted reference current can be derived as follows [3]:

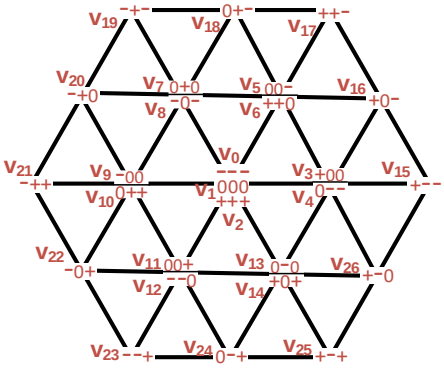

Fig. 2. Space vector representation of three level inverter

TABLE I.
SWITCHING STATE REPRESENTATION

Representation	T_1	T_2	T_3	T_4
+	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF
-	OFF	OFF	ON	ON

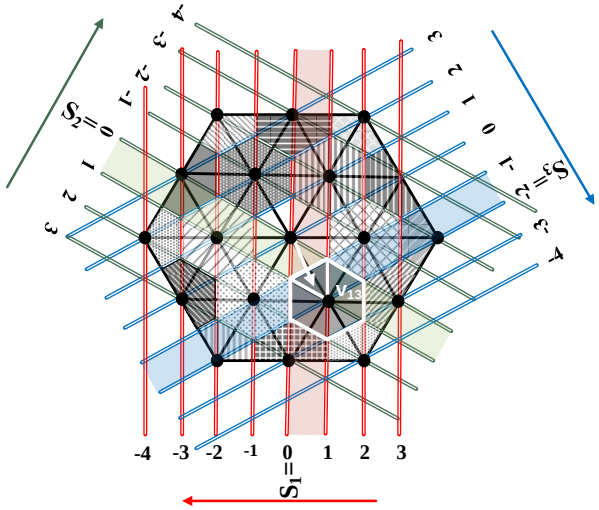

Fig. 3. Concept of 'S' factor scheme

$$\vec{v}_g(n+1) = 3\vec{v}_g(n) - 3\vec{v}_g(n-1) + \vec{v}_g(n-2) \quad (5)$$

$$\vec{i}_g^*(n+1) = 3\vec{i}_g^*(n) - 3\vec{i}_g^*(n-1) + \vec{i}_g^*(n-2) \quad (6)$$

Likewise, the predicted capacitor voltages can be obtained as follows [5]:

$$v_{c1}(n+1) = v_{c1}(n) + \frac{T_s}{C_1}i_{c1}(n) \quad (7)$$

$$v_{c2}(n+1) = v_{c2}(n) + \frac{T_s}{C_2}i_{c2}(n) \quad (8)$$

After predicting all the desired variables using (4-8), the following procedure can be followed to accomplish NPV control and grid current control of the NPC inverter.

The space vector representation of three-level NPC is depicted in Fig. 2 and the corresponding SS are enumerated in Table I. The set of SS of the NPC can be divided into two

categories, viz. redundant SS (v_0 to v_{14}) and non-redundant SS (v_{15} to v_{26}). The redundant SS can be further divided into two categories, viz. zero redundant SS (v_0 to v_2) and Non-Zero Redundant (NZR) SS (v_3 to v_{14}). Zero SS do not affect the NPV and produce zero line to line voltage [17]. Therefore, any one of the zero SS can be selected.

Likewise, each pair of NZR SS produces an equal line to line voltage. However, the current direction flowing into the neutral point is the opposite. Out of all the NZR SS, the positive NZR SS (v_3, v_6, v_7, v_{10}, v_{11} and v_{14}) increase the NPV (v_{c2}) and the negative NZR SS (v_4, v_5, v_8, v_9, v_{12} and v_{13}) decrease the NPV. Therefore, the NPV balance can be performed with a suitable selection of NZR SS [17] depending upon the predicted capacitor voltages. Since the non-redundant SS are not used in achieving NPV balance, the THD of the grid current remains unaffected.

After selecting suitable nineteen SS out of twenty-seven SS for accomplishing the voltage balancing task, the next step is to determine the optimal switching state which gives the minimum cost function for controlling the grid current. The cost function for controlling the grid current is given by [11-15]:

$$g(n+1) = \left\| \vec{v}^{*}_{inv}(n+1) - \vec{v}_{inv}(n+1) \right\|^2 \tag{9}$$

The above cost function signifies the square of the distance between two vectors. Minimization of the given cost function can be alternatively done by finding the optimal voltage vector which is close to the PRIV vector ($\vec{v}^{*}_{inv}(n+1)$). In this paper, this objective is achieved by using a novel scheme, which takes the advantages of the geometry and the space vector diagram of multilevel inverters to obtain the optimal voltage vector.

In this scheme, three imaginary lines S_1, S_2 and S_3 slide along the direction as shown in Fig. 3 and take only the marked integral positions [16]. For example, if the values of sliding lines are taken as S_1 =0.3, S_2 = 0.4 and S_3 = -1.3, they will slide to take the position of S_1 =0, S_2 =0 and S_3 = -2, which are the nearest integers less than their real values. The direction of sliding motion of S_1, S_2, and S_3 is inclined at 180^0, -60^0 and 60^0 respectively with respect to the x-axis. These three imaginary sliding lines have two interesting features, which are discussed next, and by virtue of these, the calculation burden in FCSMPC is reduced.

The first feature is that considering all the integral positions of the three imaginary sliding lines; it can be noticed from Fig. 3 that every possible switching state of the three-level inverter (marked by black dots) are separated from one another by its optimal area (highlighted by different patterns). It can be seen that every optimal area has only one switching state. The optimal area of a switching state is so called because if the PRIV vector falls in that area, it will be closest to that switching state. Therefore, that switching state can be taken as the optimal switching state. Hence, if the optimal area where the PRIV vector lies is located, the optimal switching state can be easily found out.

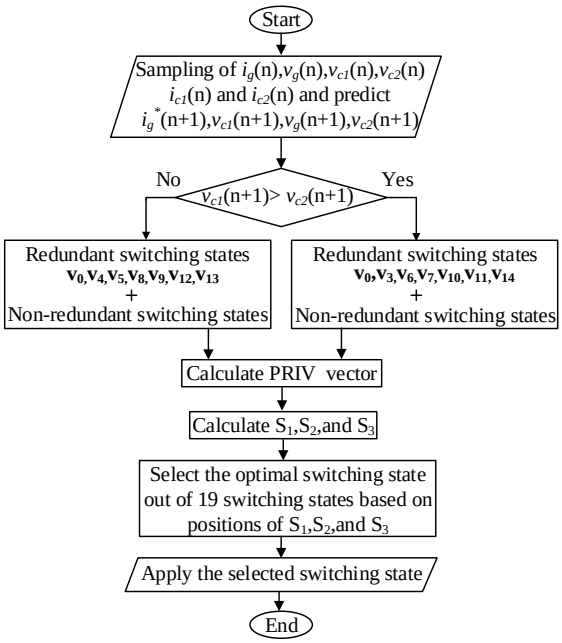

Fig. 4. Algorithm for the 'S' factor scheme based FCSMPC.

$$\left.\begin{aligned} S_1 &= \left(1/V_{DC}\right)\left(4v^{*}_{invx}(n+1)\right); \\ S_2 &= \left(1/V_{DC}\right)\left(-2v^{*}_{invx}(n+1) - 6v^{*}_{invy}(n+1)/\sqrt{3}\right); \\ S_3 &= \left(1/V_{DC}\right)\left(-2v^{*}_{invx}(n+1) + 6v^{*}_{invy}(n+1)/\sqrt{3}\right) \end{aligned}\right\} \tag{10}$$

The second interesting feature is that if the values of the three imaginary lines for the inverter are obtained by using (10), they will always enclose the tip of PRIV vector within a triangle, which is a part of an optimal area. The positions of sliding lines can be obtained from the values of sliding lines by using a floor function. For example, if the PRIV vector is the vector shown by an arrow in Fig. 3, the position of S_1, S_2 and S_3 can be calculated as 0, 0 and -2 respectively from (10). This implies that the PRIV vector is enclosed in a triangle, which is a part of the optimal area of v_{13}/ v_{14}. Therefore, once the positions of S_1, S_2, and S_3 are obtained, one can easily find out the optimal switching state. Since three imaginary lines slide along three different directions to locate the optimal switching state, this scheme has been called the 'S' factor scheme. The step by step procedure to implement the proposed scheme is given in the form of a flow chart as shown in Fig. 4.

Neural point voltage and grid current may also be controlled in any '*m*'level inverter following the same procedure with slight modification in the calculation procedure of S_1, S_2, and S_3 and suitable selection of redundant SS. The generalized expressions for S_1, S_2, and S_3 for an '*m*' level inverter are given as follows:

$$\left.\begin{aligned} S_1 &= \left(1/V_{DC}\right)\left(2(m-1)v^*_{invx}(n+1)\right); \\ S_2 &= \left(1/V_{DC}\right)\left(-(m-1)v^*_{invx}(n+1) - 3(m-1)v^*_{invy}(n+1)/\sqrt{3}\right); \\ S_3 &= \left(1/V_{DC}\right)\left(-(m-1)v^*_{invx}(n+1) + 3(m-1)v^*_{invy}(n+1)/\sqrt{3}\right) \end{aligned}\right\} \quad (11)$$

III. Experimental Results

The hardware validation of the proposed scheme for NPV control and grid current control was carried out on a 500W three-level NPC inverter. Redundant SS are also used to balance NPV in the conventional sector distribution based MPC [14] to have a fair comparison. The sector identification method followed to implement the conventional algorithm is given in [18]. The specifications of the hardware set-up are enumerated in Table-II. The DSP processor TMS320F28335 is used to implement the control algorithms. The execution time is recorded by using an output pin, which is set to '1' at the beginning of the algorithm and reset to '0' at the end of the algorithm.

The static and dynamic performance analysis and total harmonic distortion (THD) analysis have been carried out for the two algorithms. The step change in grid current and the magnified view of the transient response (rise time) while active power is changed from 200W to 500W in the conventional algorithm is shown in Fig. 5. The corresponding grid current waveforms and their magnified view with the proposed 'S' factor scheme based FCSMPC for an identical step change of power are shown in Fig. 6. It can be observed that the rise time for both the schemes is almost equal. The data of active power waveforms are taken from the code composer studio and plotted in Matlab to examine the steady-state error with the two algorithms. The active power waveforms of the two algorithms are shown in Fig. 7. It is evident that power is regulated with a very low steady-state error in both the algorithms. The THD of both the schemes is found to be very close at around 2.3%. The NPV balancing has been performed in both the schemes and the results are shown in Fig. 8. It is evident that both the conventional and the proposed scheme give similar performance and only redundant SS are enough for carrying out NPV balancing.

From the above discussion, it is observed that the static and dynamic performances of the proposed 'S' factor scheme based FCSMPC and the conventional FCSMPC do not have a significant difference between them. The execution times of the two schemes are shown in Fig. 9. It is clear that the execution time of the proposed 'S' factor scheme shown in Fig. 9(a) is 3.7µs, which is almost 70% lower than the execution time of the conventional method shown in Fig. 9(b).

TABLE II.
System Specifications

Parameters	Value	Unit
Grid frequency	50	Hz
Sampling time (T_S)	50	µs
DC link capacitors (C_1,C_2)	1000	µF
Parasitic resistance (R)	.4	Ω
DC link voltage	150	V
Inductor(L)	4	mH

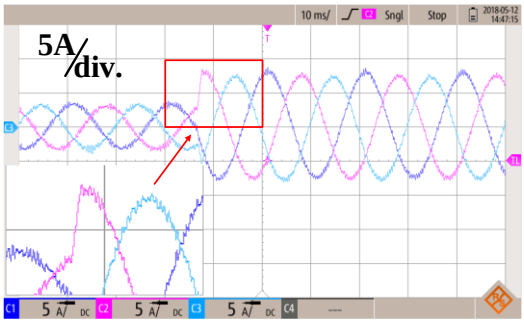

Fig. 5. Experimental results for step change in grid current in conventional scheme

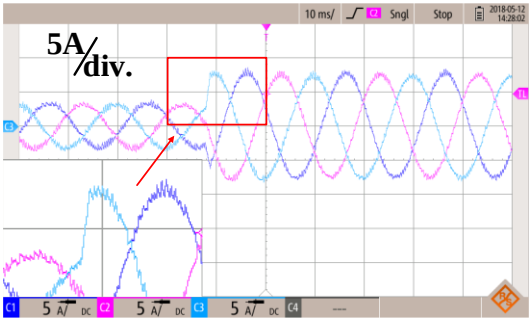

Fig. 6. Experimental results for step change in grid current in proposed scheme

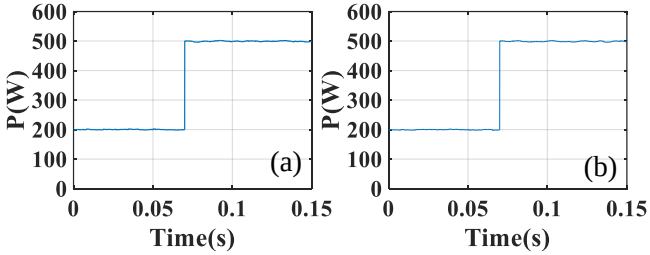

Fig. 7. Active power regulation with the two schemes: (a) Proposed scheme; (b) Conventional scheme

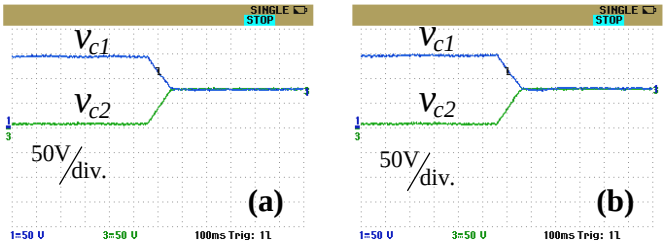

Fig. 8. NPV balance: (a) proposed scheme; (b) Conventional scheme

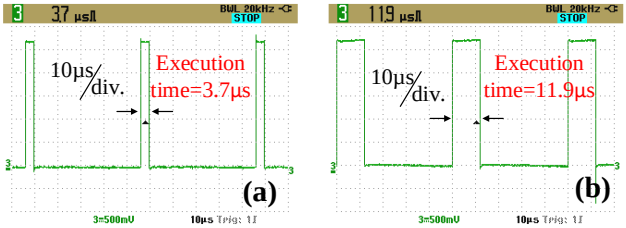

Fig. 9. Execution time: (a) proposed scheme; (b) Conventional scheme

IV. Conclusion

This paper has reported a novel FCSMPC algorithm based on the proposed 'S' factor scheme for grid-tied three-level NPC inverter. Three imaginary sliding lines, which isolate every switching state from one another reduced the complexity in the FCSMPC. Therefore, FCSMPC can be easily applied to any higher level inverter with the help of the proposed scheme and the knowledge of the space vector diagram. The proposed scheme was evaluated experimentally for a three-level inverter, and the experimental results were compared with a recent FCSMPC algorithm to demonstrate the superiority of the proposed scheme. It was proved that this scheme is capable of controlling both the grid current and the NPV efficiently without evaluating any cost functions. The THD of the grid current remained unaffected since only redundant SS were used for voltage balancing. It was also observed that the performance of the proposed scheme remains comparable to that of the conventional FCSMPC algorithm. However, this scheme reduces the execution time of the FCSMPC by approximately 70% as compared to the conventional algorithm thereby reducing the computational burden. Since the number of cost functions increases for higher level inverters, it is expected that the execution time will also be higher with conventional FCSMPC. Therefore, with the proposed algorithm, the percentage of reduction in execution time can be reduced further in higher level inverters.

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